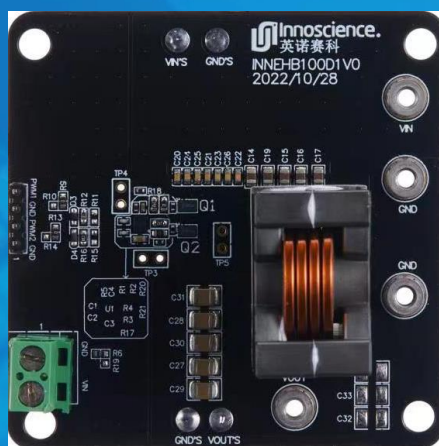


INNEHB100D1

Evaluation Board Manual

100V GaN HEMT INN100W070A
Open Loop Half-Bridge EVB





CAUTION

Please carefully read the following content since it contains critical information about safety and the possible hazard it may cause by

ELECTRICAL SHOCK HAZARD

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.

Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

HOT SURFACE

The surface of PCB can be hot and could cause burns. DO NOT TOUCH THE PCB WHILE OPERATING!!

REMINDER

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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1. Overview

1.1. Introduction

INNEHB100D1 is a half-bridge evaluation board equipped with the half-bridge gate driver to evaluate the performance of 100V GaN HEMT INN100W070A. This board can simplify the test process, it can easily realize Buck converter with single or dual PWM input. The evaluation board can be used in BUCK circuit frequency range of 400KHZ to 800KHZ, input voltage range of 36V to 80V, under the frequency of 600KHZ and the wind speed of 1400LFM, 48V-12V full load 15A efficiency can reach 96.25%. The board can be used not only for BUCK circuits, but also for BOOST circuits. The board includes all the necessary information you need, and the layout has been optimized to achieve the best performance. Test points are also included for the waveform measurement and efficiency evaluation.

1.2. Test Equipment Requirement

To evaluate the performance properly, you need to prepare the following test equipment:

- 1) High speed digital oscilloscope ($\geq 500\text{MHz}$ Bandwidth)
- 2) Two Low voltage DC power supply
- 3) PWM generator
- 4) Digital Multimeter
- 5) DC load (E-load or Power Resistor)

2. Performance summary

Table 1 Electrical Characteristic (Ta=25°C)

Symbol	Parameters	Min	Nom	Max	Units
VDD	VDD supply Voltage	7	8	12	V
Vin	Input Voltage	36	48	80 ⁽¹⁾	V
Fsw	Switching frequency		600		KHZ
Pout	Output Power			204 ⁽²⁾	W
EFF	Typical efficiency		96.25% ⁽³⁾		
Vpwm	Input Logic 'High'	3.5		5	V
	Input Logic 'Low'	0		1.5	V

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 100 V for INN100W070A.

(2) Maximum output power will be subject to switching frequency, bus voltage, load current EVB temperature and thermal cooling.

(3) 96.25% is the efficiency at 48V to 12V, load 15A, frequency 600KHZ, and the wind speed of 1400LFM.

3. Block Diagram

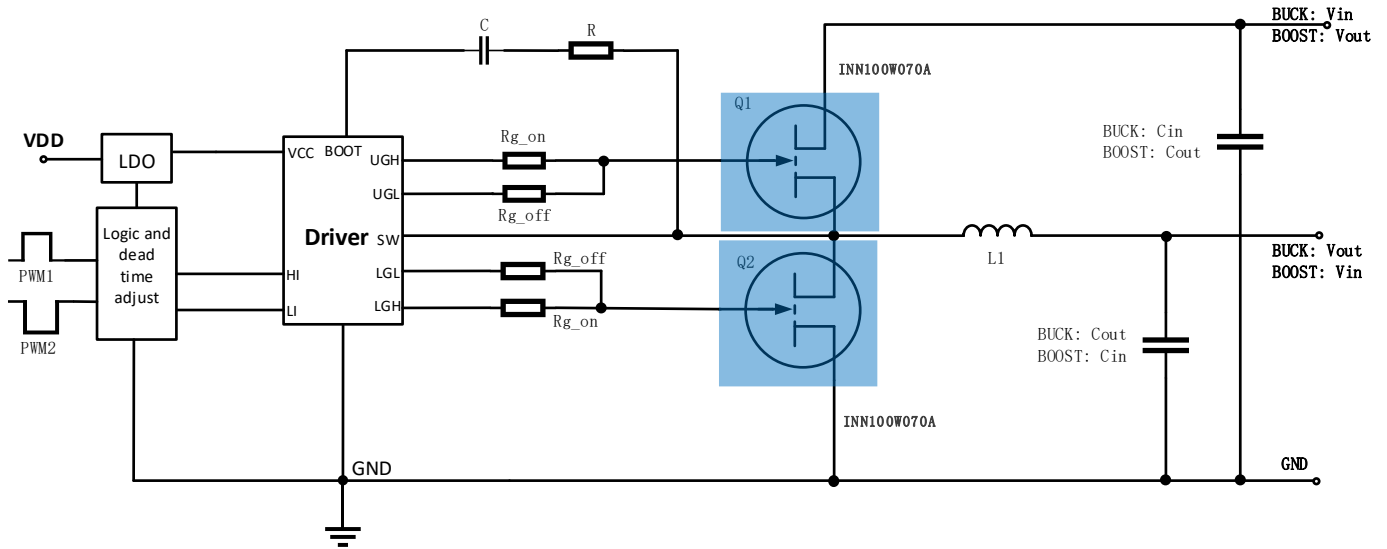


Figure 1 INNEHB100D1 Block Diagram

4. EVB Overview and Schematic

4.1. EVB Overview

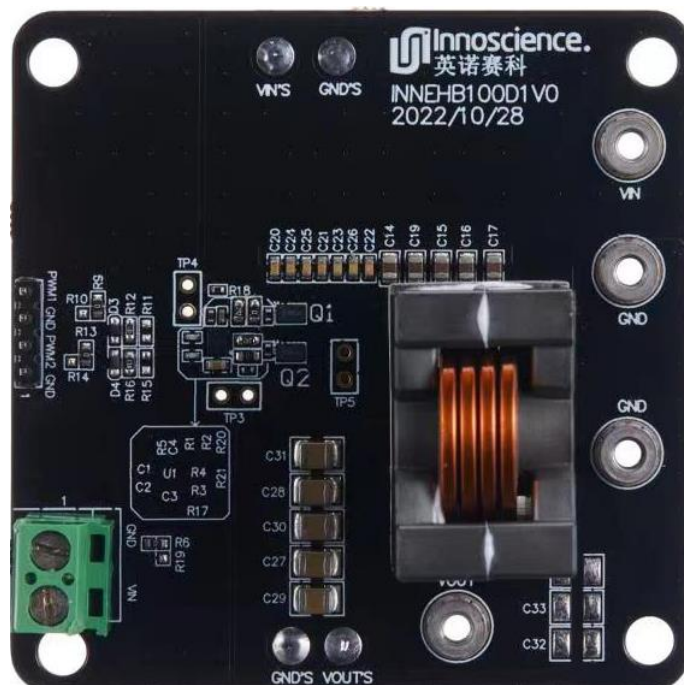


Figure 2 Top view of INNEHB100D1

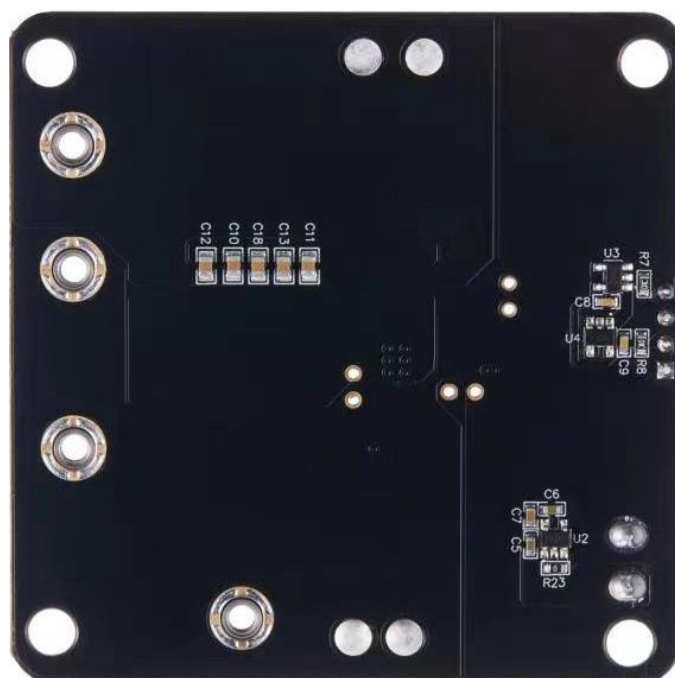


Figure 3 Bottom view of INNEHB100D1

4.2. Schematic

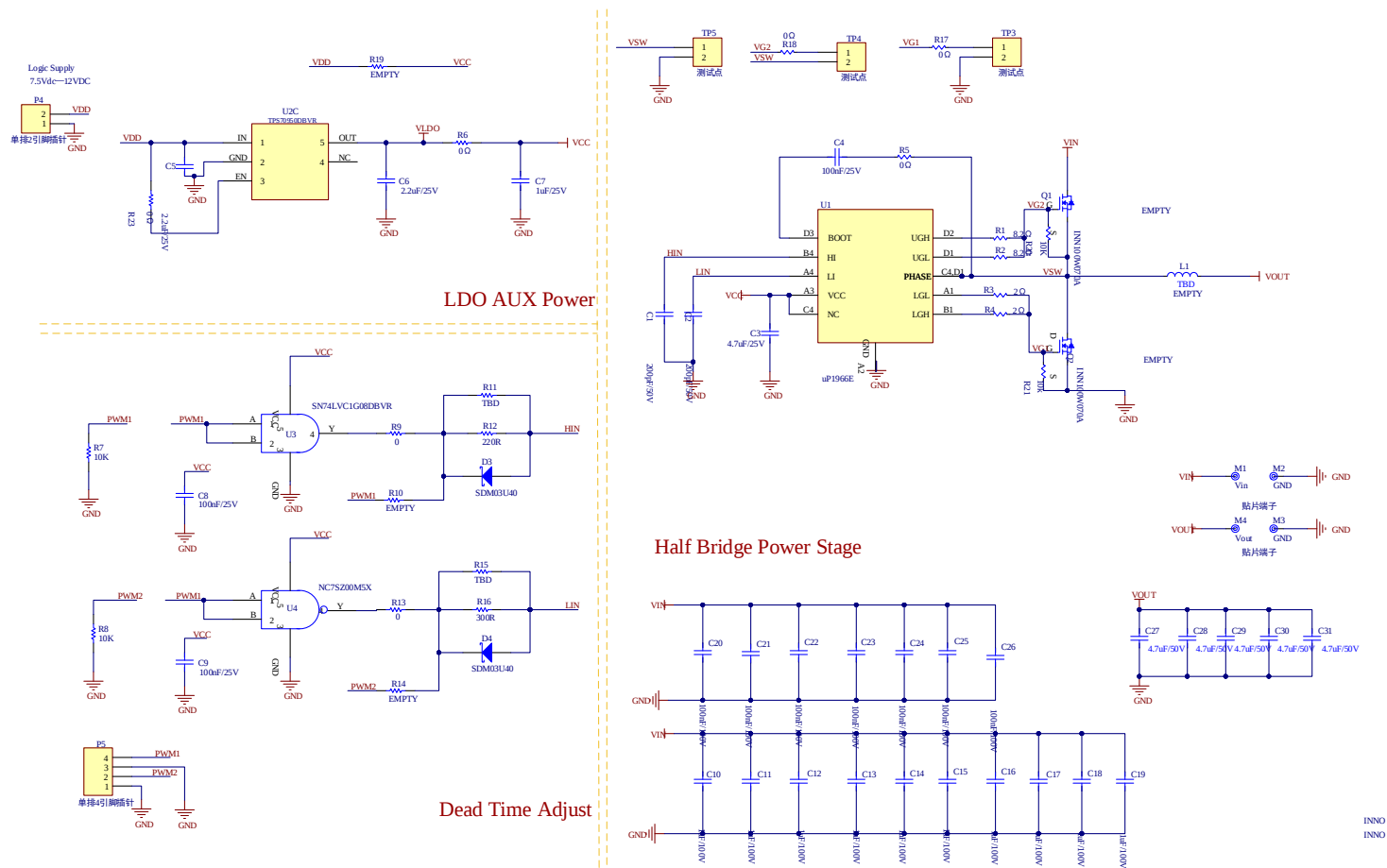


Figure 4 Schematic

5.1. Test point location



5.2. Test setup

5.2.1. Buck Mode



Figure 6 Single-PWM input Buck mode

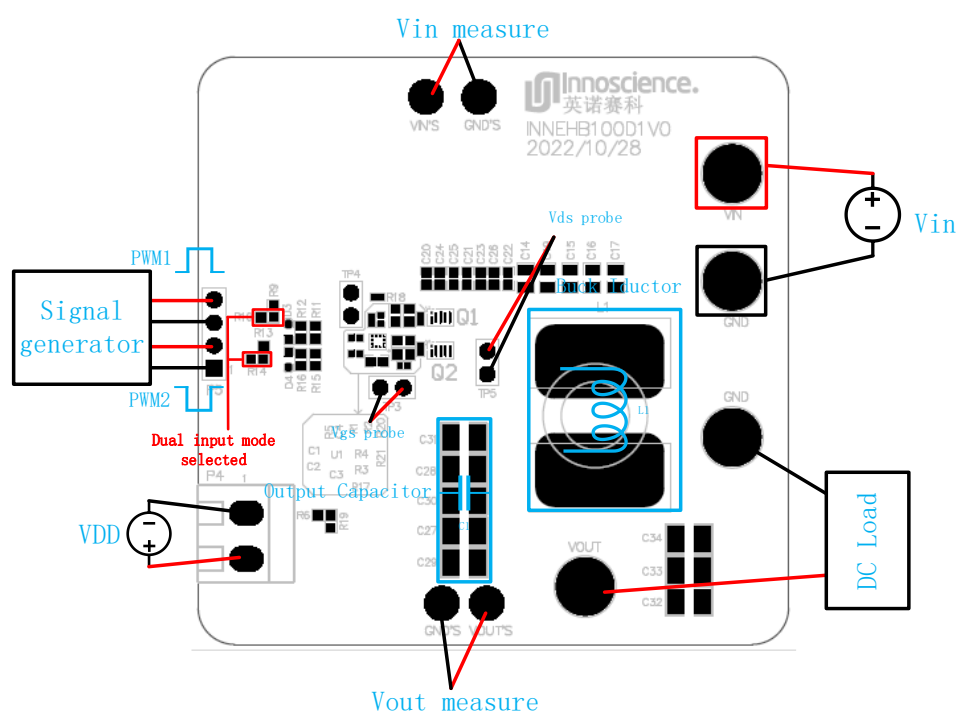


Figure 7 Dual-PWM input Buck mode

Before tests, single or dual PWM input modes could be selected. When selecting the single PWM input mode, please solder 0Ω resistor to R9 & R13. The dead time is regulated by R12, R16, C1 and C2. The value for R12 is 220Ω , and R16 is 300Ω . The value of C1 and C2 is 200 pF . At this time, at the load of 10 A , the corresponding measured dead time between lower FET shutdown and upper FET opening is about 10 ns , and the dead time between upper FET shutdown and lower FET opening is also about 10 ns .

To select dual PWM mode, please solder 0Ω resistor to R10, R14, R12 and R16. Figure 7 Dual-PWM input Buck mode shows the required PWM signals; PWM1 and PWM2 should be complementary. The dead time is controlled by the signal generator.

5.2.2. Boost Mode

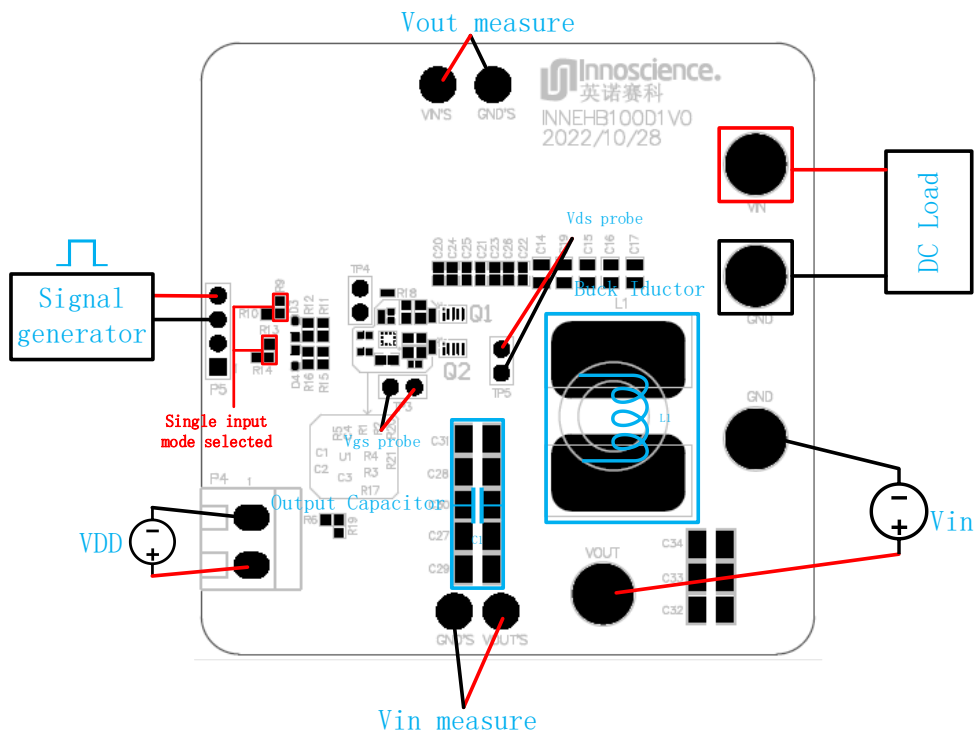


Figure 8 Single-PWM input Boost mode

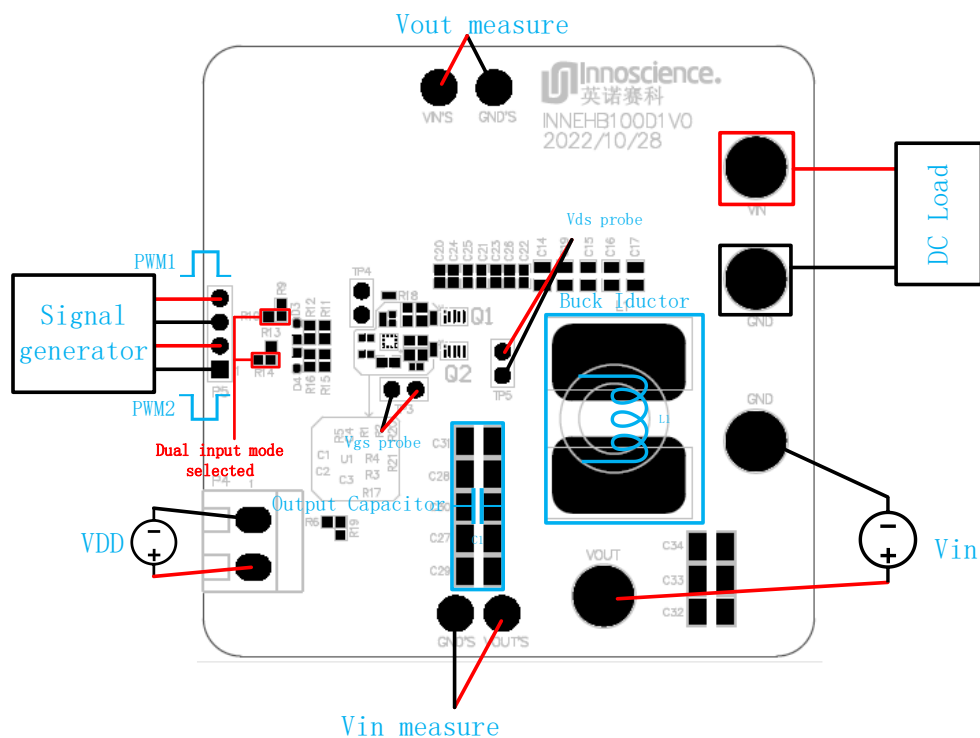


Figure9 Dual-PWM input Boost mode

5.3. Power up and down sequence

5.3.1. Power-up sequence (Buck Mode)

1. Check every power supply is **off**.
2. Connect the DC voltage source to terminal **VIN** and common ground terminal **GND**, as shown in Figure 6 (Pay attention to the polarity).
3. Connect the electronic load to pin **VOUT**.
4. Connect the auxiliary source to the VDD terminal **P4** (Pay attention to the polarity).
5. Connect the signal generator to pin **P5**.
6. Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.
7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.
8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Probe switch-node and view the switching operation.
9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

5.3.2. Power-up sequence (Boost Mode)

1. Check every power supply is **off**.
2. Connect the DC voltage source to pin **VOUT**, as shown in Figure 8 (Pay attention to the polarity).
3. Connect the positive pole of the electronic load to pin **VIN** and the negative pole to pin **GND**.
4. Connect the auxiliary source to the VDD terminal **P4** (Pay attention to the polarity).
5. Connect the signal generator to pin **P5**.

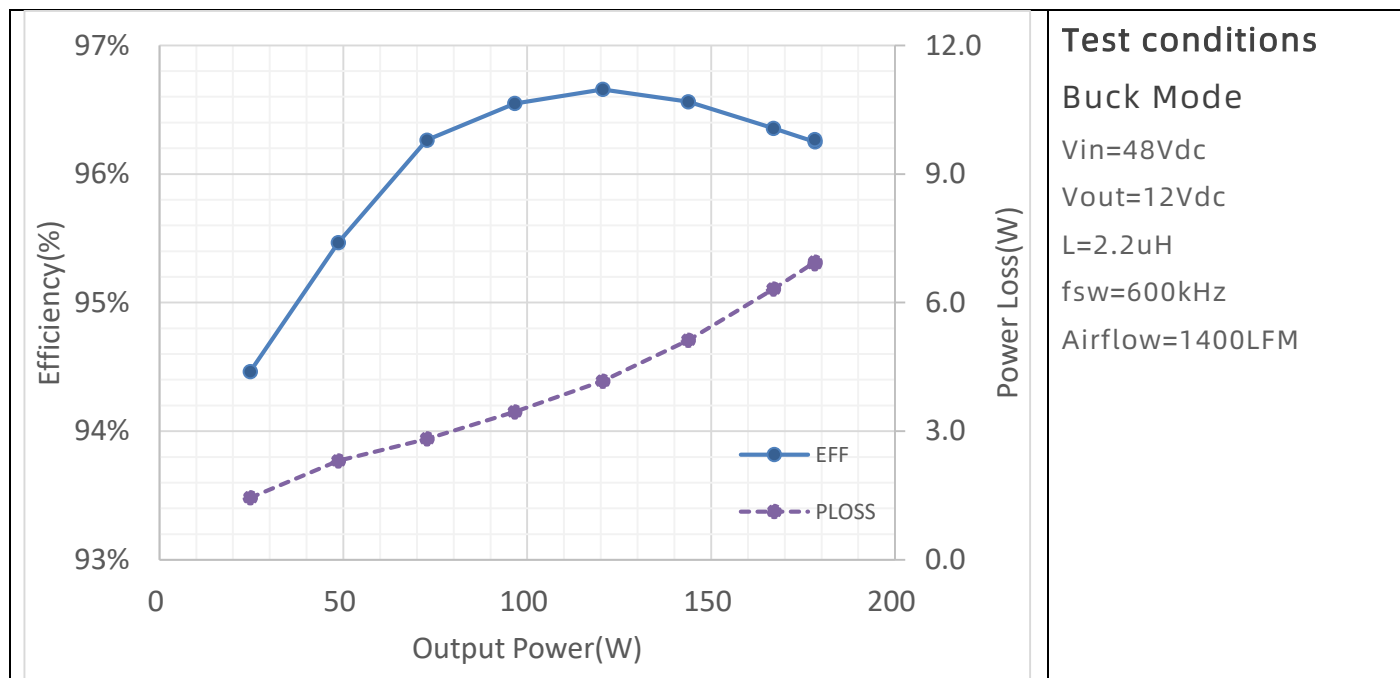
6. Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.
7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.
8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (do not exceed the absolute maximum voltage). Probe switch-node and view the switching operation.
9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

5.3.3. Power-down sequence

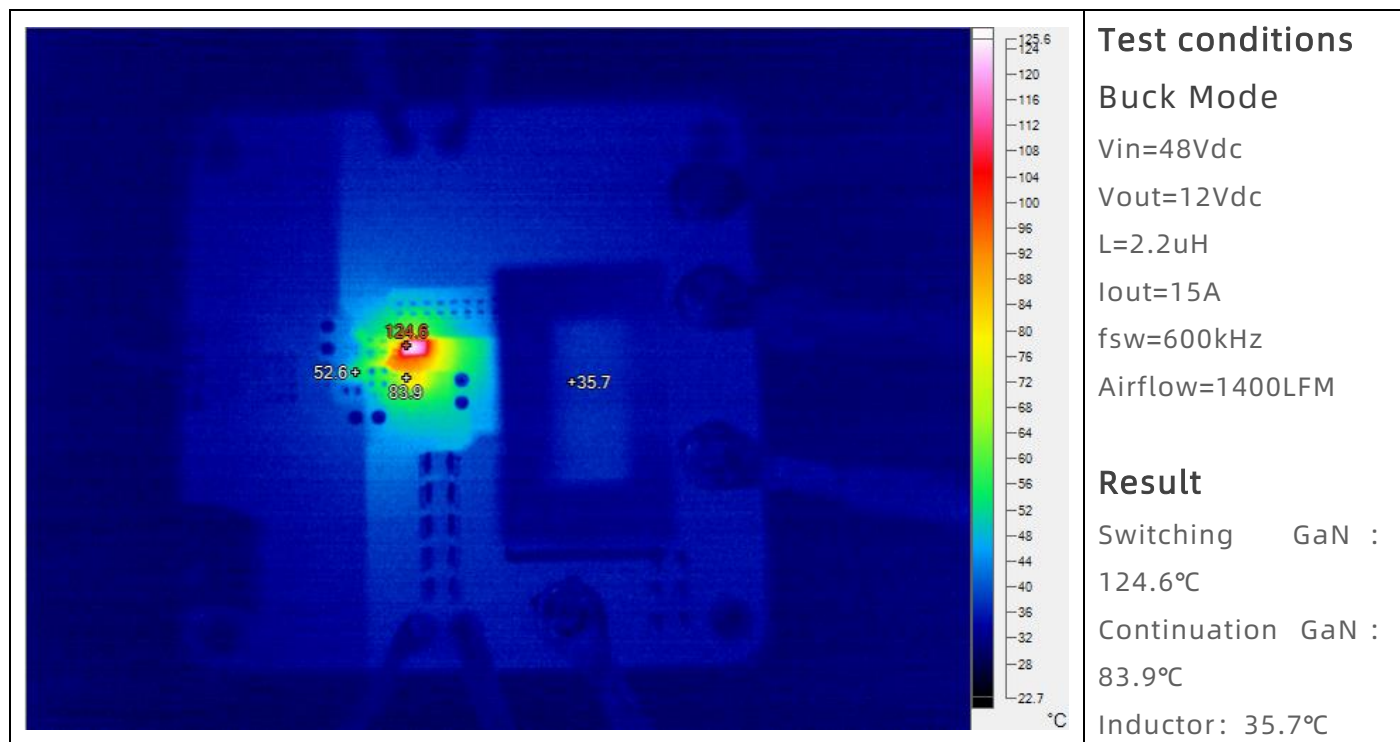
1. Turn off the **E-load** first
2. Turn off the **DC voltage source**
3. Turn off the **PWM generator**
4. Turn off the **auxiliary power supply**

6. Evaluation Results

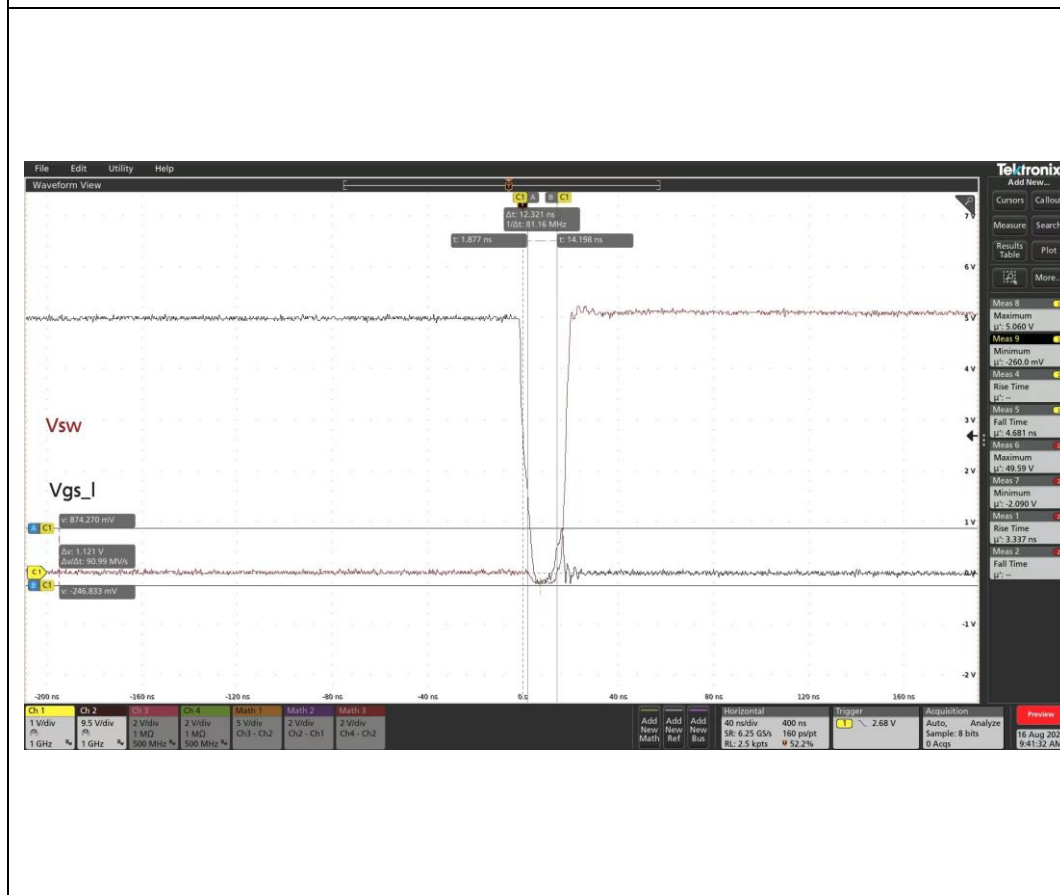
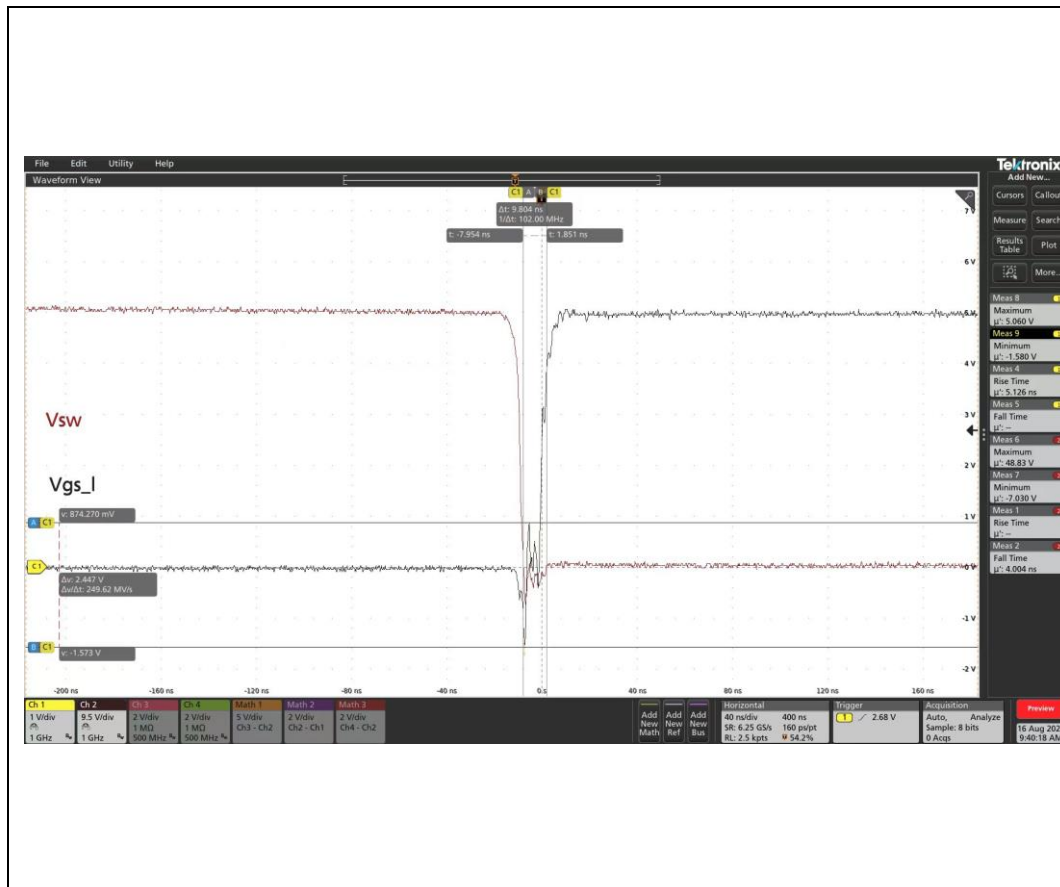
6.1.1. Efficiency Results



6.1.2. Thermal performance



6.1.3.Switching Waveforms



Appendix

Appendix A. PCB Layout

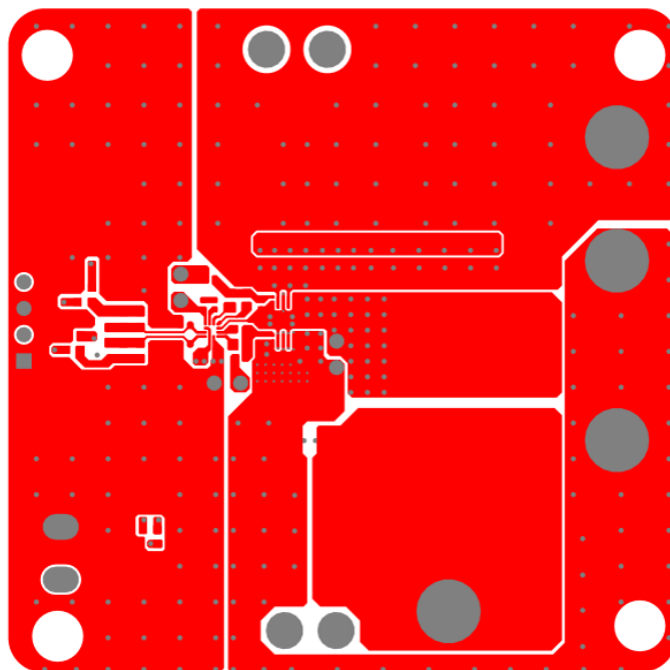


Figure 10 The top layer of INNEHB100D1

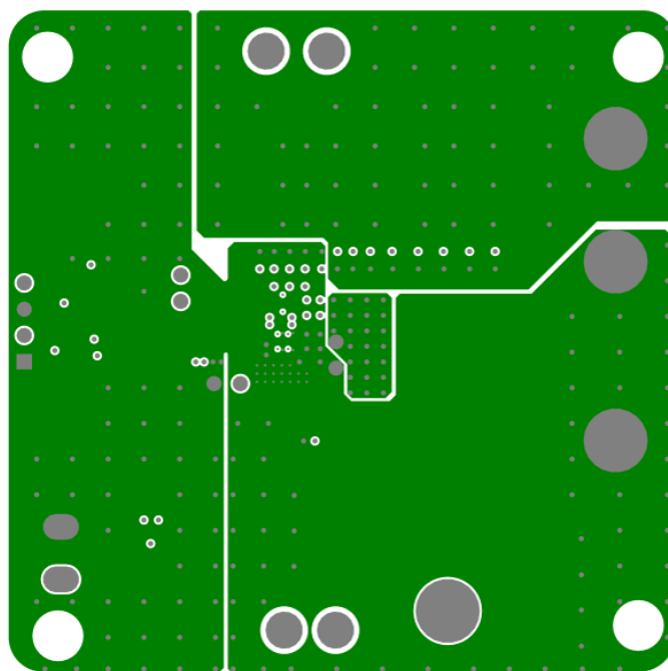


Figure 11 The first middle layer of INNEHB100D1

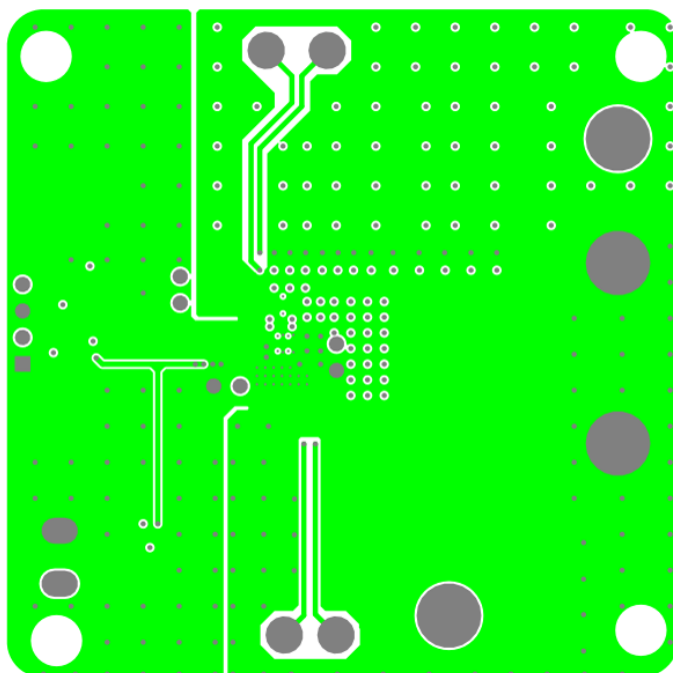


Figure 12 The second middle layer of INNEHB100D1

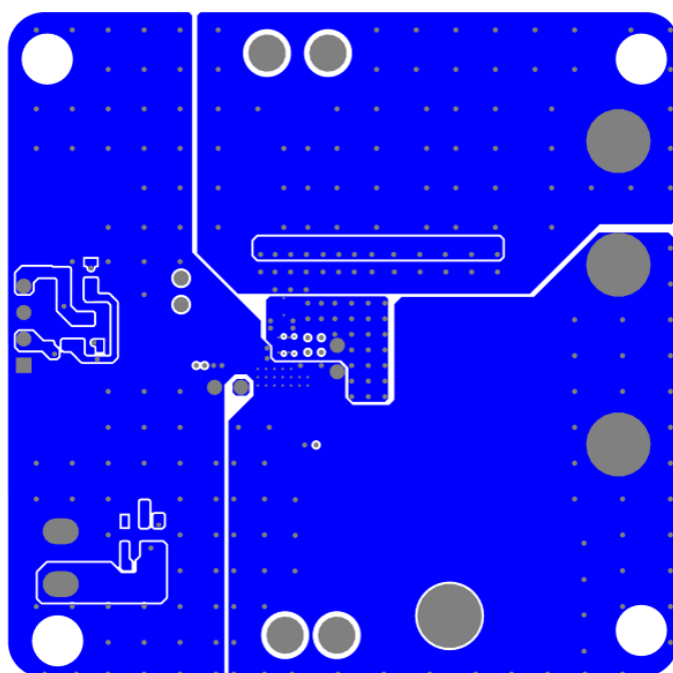


Figure 13 The bottom layer of INNEHB100D1

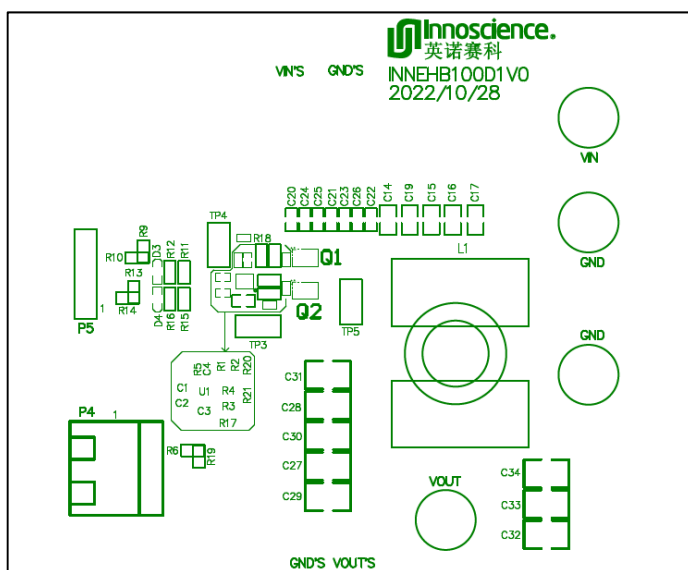


Figure 14 The top overlay of INNEHB100D1

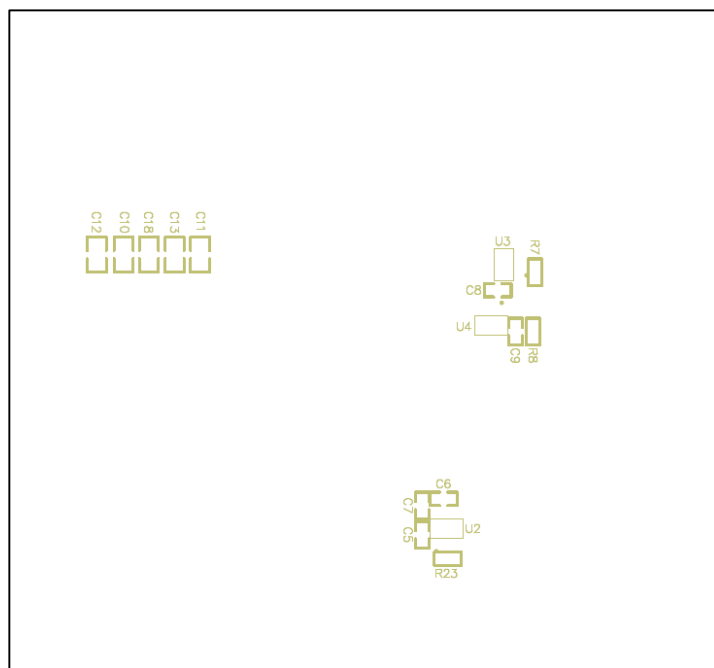


Figure 14 The bottom overlay of INNEHB100D1

Appendix B. BOM

Table 2 BOM

Designator	Part Number	Manufacturer	Description	Footprint	Quantity
C1, C2	CC0402JRNPO9BN201	YAGEO	Cap, 200pF, COG, 50V, ±5%,	C0402	2
C3, C5, C6, C7	GRM188R61E225KA12D	MURATA	Cap, 2.2uF, X7R, 25V, ±10%	C0603	4
C4	0402B104K250CT	WALSIN	Cap, 100nF, X7R, 25V, ±10%	C0402	1
C8, C9, C20, C21, C22, C23, C24, C25, C26	CL10B104KC8NNNC	SAMSUNG	Cap, 100nF, X7R, 100V, ±10%	C0603	9
C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	HMK212BC7105KGHTE	TAIYO YUDEN	Cap, 1uF, X7R, 100V, ±10%	C0805	10
C27, C28, C29, C30, C31	CL32B475KBJNFNE	SAMSUNG	Cap, 4.7uF, X7R, 50V, ±10%	C1210	5
C32, C33, C34	EMPTY		Cap	C1210	3
R6, R9, R13, R23	0603WAF0000T5E	UNI-ROYAL	Res, 0R, 1%, 0.1W	R0603	4
R1,R2	0603WAF820KT5E	UNI-ROYAL	Res, 8.2R, 1%, 0.1W	R0603	2
R3,R4	WR06W2R00FTL	WALSIN	Res, 2R, 1%, 0.1W	R0603	2
R5, R17, R18	RTT0200000FTH	RALEC	Res, 0R, 1%	R0402	3
R7, R8	0603WAF1002T5E	UNI-ROYAL	Res, 10k, 1%, 0.1W	R0603	2
R10, R11, R14, R15, R19	EMPTY		Res	R0603	5
R12	0603WA2200T5E	UNI-ROYAL	Res, 220R,1%,0.1W	R0603	1
R16	0603WAF3000T5E	UNI-ROYAL	Res, 300R,1%,0.1W	R0603	1
R20, R21	0402WGF1002TCE	UNI-ROYAL	Res,10K,1%,0.063W,0402	R0402	2
L1	EMPTY		Inductance	R0603	1
D3, D4	SDM03U40-7	DIODES	Schottky, 30V, 30mA	SOD-523	2
Q1, Q2	INN100W070A	INNOSCIENCE	GAN FETs, 100V/7mΩ	FCSP 2.6mm×1.6mm	2
U1	uP1966E	UPI SEMICONDUCTOR	Dual-Channel Gate Driver	WLCSP1.6x1.6-12B	1
U2	TPS70950DBVR-TP	TECH PUBLIC	LDO voltage regulators , fixed 5V output,	SOT-23	1
U3	SN74LVC1G08DBVR	TEXAS INSTRUMENTS	Single 2-Input Positive-AND Gate	SOT-23	1
U4	NC7SZ00M5X	ONSEMI	Two-Input NAND Gate	SC-74A	1

Revision History

Date	Author	Versions	Description	Check
17/8/2023	YubinHuang	1.0	First edition	AE Team



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